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Effect of CdSe nanoparticles in polymethylmethacrylate tunneling layer on the performance of nonvolatile organic memory device

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ABSTRACT

Organic memory devices based on CdSe nanoparticles (NPs) embedded in polymethylmethacrylate (PMMA) insulating layer are demonstrated. The use of NPs/polymer blend as a tunneling layer for non-volatile organic memory has proven to be an alternative route to manipulate and improve the device characteristics. The memory effect is adjustable upon changing the concentration of CdSe NPs within the PMMA tunneling insulator, and the tunable device performance is ascribed to the different trap densities in floating gate. The capacitance change is analyzed by monitoring the charge transport between pentacene and the CdSe NPs. Our in-depth study reveals that the increase in CdSe NPs leads to a wider memory window and better hysteresis characteristics with a maximum window of −8.6 V at V_{GS} of −30 V for 1 s. This result demonstrates the potential application of organic/inorganic hybrid floating gate structure in organic memory devices.

1. Introduction

The development of memory device technology has been driven towards the fabrication of low-cost, high-density, and non-volatile solid state of devices [1–5]. Among various non-volatile memory devices, organic memory devices have been intensively investigated over the last decade due to their attractive features such as low-cost, low-temperature processibility and mechanical flexibility [6–10]. The operation of organic memories typically relies on three concepts: resistive switching, polymer ferroelectric, and charge-storage in dielectric. The resistive switching organic memory was developed by the Yang group [11,12]. A nonvolatile plastic digital memory device based on the nanofibers of the conjugated polymer polyaniline decorated with gold nanoparticles is reported. ON–OFF switching time of less than 25 ns is observed. The devices possess prolonged retention time of several days after they have been programmed. The integration of ferroelectrics for organic nonvolatile memory has attracted much attention. Kang and coworkers [13] demonstrated significantly improved performance of a nonvolatile polymeric ferroelectric field effect transistor (Fe-FET) memory using nanoscopic confinement of poly(vinylidene fluoride-co-trifluoroethylene) (PVDF-TrFE) within self-assembled organosilicate (OS) lamellae. This device has a programming voltage as low as ±8 V and data retention of ~2 h. Also several types of gate dielectrics enable reversible trapping of charges upon application of a gate field, for instance polymer electrets [14], dielectrics with embedded metallic [15] or semiconducting nanoparticles (NPs) [16] with permanent and/or switchable electrical dipoles. Each of these memory devices has potential, but remaining issues also has to be solved.

Among these technologies, organic memories based on NPs have attracted a great deal of interest because of their potential applications in next-generation memory devices. In these device structures, a relatively large conventional floating gate is replaced with a two-dimensional array of small, nano-scaled particles embedded in the insulator. This structural configuration is beneficial for charge storage devices in terms of better retention, which allows for thinner tunnel insulator and thus results in lower operating voltages. Further, this characteristic shortens channel length with reduced punch-through (consequently reducing the cell area) and suppresses leakage current [17,18]. In general, metal NPs such as Au, Ag, and Cu have been utilized as charge-trapping elements for non-volatile memory devices [15,19,20]. In comparison to the

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metal NPs-based memory devices, the devices using semiconductor NPs as charge traps possess many intriguing properties and are therefore a powerful tool for the development and fabrication of materials with novel functions. Most of the researches on the fabrication of NPs-based memory device have focused on the development of self-assembled monolayers of the NPs and Langmuir–Blodgett films with NPs intervened between pentacene and dielectric. These methods, however, are inevitably subjected to complicated processes including repetitive nanoparticle adsorption steps.

Herein, we demonstrate the utilization of semiconductor NPs to tune the memory window in organic memory device. We developed a novel procedure for the fabrication of the NP-based floating gate memory with CdSe NPs dispersed in polymethylmethacrylate (PMMA) insulating layer. The unique feature of this structure is that the multilayers of CdSe NPs can be formed inside the PMMA tunneling insulator, which leads to a large memory window, potential multilevel charging characteristics, and improved retention properties.

2. Experimental

CdSe NPs were prepared by the hot injection method with some modifications [21]. CdO (0.39 mmol), trioctylphosphine oxide (5.2 mmol), and tetradecylphosphonic acid (1.1 mmol) were degassed at 110 °C for 1 h and then heated under nitrogen to 315 °C to completely dissolve the precursors. TOPSe (0.25 mmol Se dissolved in 4.25 mL of trioctylphosphine) was subsequently injected into the hot solution to initiate the reaction. After 5 min of growth at 270 °C, the NP solution was cooled to room temperature, washed three times with a mixture of methanol and toluene, and dissolved in toluene for use.

Fig. 1 shows a schematic illustration of the organic memory device and storage element configuration. The metal–insulator–semiconductor (MIS) structure was fabricated on indium–tin-oxide (ITO) glass substrate as a gate electrode. Substrates were cleaned by regular cleaning procedure: sonication followed by rinsing with acetone, isopropanol, and deionized water. A control device that excludes CdSe NPs from PMMA insulating layer was fabricated by spin coating the PMMA solution (average molecular weight 950 K, diluted in 4% anisole) twice at 4500 rpm for 60 s over ITO and subsequent baking at 160 °C for 30 min in a conventional oven. This resulted in a 400 nm thick PMMA gate insulator layer. For the fabrication of NPs based floating gate memory device, the CdSe NPs solution was first mixed with the PMMA solution. The mixed solution was spun over a predeposited PMMA layer (200 nm) and was subsequently baked at 160 °C for 30 min in an oven. The thickness of PMMA layer including CdSe NPs was 50 nm. The size of CdSe NPs was ~4.0 nm in diameter, and CdSe NP solutions with three different concentrations (7.3×10^{14}, 1.0×10^{15}, and 2.0×10^{15} particles/ml) were employed. The pentacene layer (~70 nm) was then deposited by thermal evaporation at a rate of 0.1 Å/s under high vacuum less than 5×10^{-6} torr. A top metal electrode (gold) was subsequently deposited by thermal evaporation through a shadow mask having 500 μm in diameter. The structural characterization of the cross-sectional specimen prepared by a conventional method was carried out using transmission electron microscopy (TEM, JEOL 2010F). The TEM specimen was cut out of the device by focused ion beam (FIB, NOVA 600 Nanolab) and was transferred to a copper grid [22]. The electrical properties of devices were analyzed by capacitance–voltage (*C–V*) characteristics at room temperature under ambient condition using HP 4284A LCR meter at a frequency of 100 kHz.

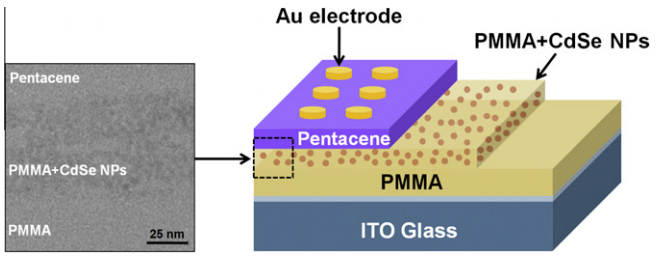

Fig. 1. Schematic illustration of memory architectures and cross-sectional TEM image of the fabricated device featuring CdSe NPs embedded in PMMA layer.

3. Results and discussion

Fig. 1 shows a cross-sectional TEM image of our device, which clearly shows that CdSe NPs were uniformly embedded in PMMA layers without aggregation. To investigate the performance of CdSe NP-embedded memory device, the control device was first examined. The MIS control sample fabricated without the use of CdSe NPs displayed hysteresis-free *C–V* characteristics (Fig. 2), where the hysteresis is defined as a shift in the capacitance (ΔC). The *C–V* analysis of the control device showed no hysteresis when the gate voltage (V_{GS}) was swept from 10 to −10 V and then back to 10 V. Even when the sweeping V_{GS} was increased up to ±30 V, no hysteresis was observed, indicating the absence of any charge trapping events inside PMMA and its interface.

In contrast, hysteresis loops in counterclockwise direction were observed in the memory device containing CdSe NPs while sweeping V_{GS}. Fig. 3 displays the *C–V* curves, measured at 100 kHz, of the ITO/PMMA/CdSe NPs embedded in the PMMA/pentacene/Au device with CdSe NP concentrations of 7.3×10^{14}, 1.0×10^{15} and 2.0×10^{15} particles/ml. All three devices clearly showed counterclockwise hysteresis behavior, which is an essential feature of a bistable memory device. The *C–V* curve shifted to negative direction, which indicates that CdSe NPs were positively charged due to negative V_{GS}. This negative shift found during the application of $-V_{GS}$ implies that holes are transferred from the pentacene layer to CdSe NPs. It should be noted that no such shift was observed when the gate voltage was swept from positive to negative direction. This indicates that positive charging of CdSe NPs was more efficient than their negative charging on this device. Fig. 3d is the schematic illustration of energy band structure of our device. When a sufficiently large electric field was applied (negative V_{GS}), holes can tunnel into the valence band of the CdSe NPs from the highest occupied molecular orbital (HOMO) level of the nearby pentacene molecules. The injected holes can remain confined within the CdSe NPs even after the negative V_{GS} was removed.

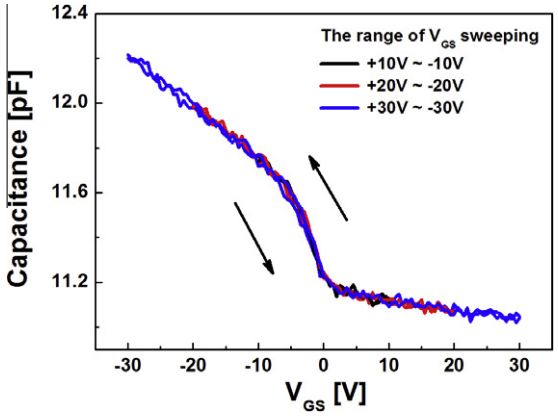

Fig. 2. The *C–V* characteristic of the organic memory without CdSe NPs. (PMMA/PMMA insulator).

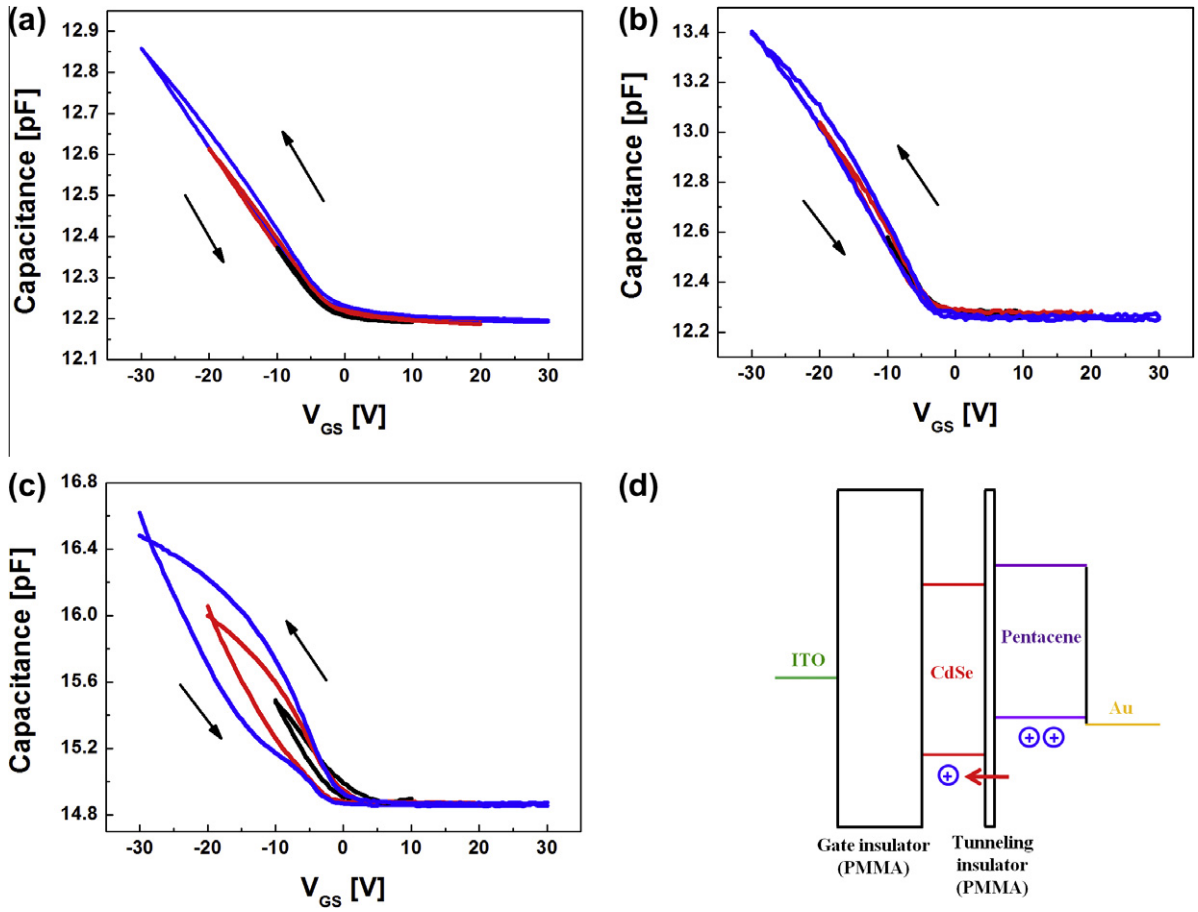

Fig. 3. The *C–V* characteristic of the fabricated organic memory with different concentrations of CdSe NPs at different V_{GS} sweeping range, (a) 7.3×10^{14}, (b) 1.0×10^{15}, (c) 2.0×10^{15} particles/ml. (d) Schematic illustration of the energy band structure of the organic memory without CdSe NPs.

The capacitance shift (ΔC) in the device increases linearly with the increase of CdSe NP concentration from 7.3×10^{14} to 2.0×10^{15} particles/ml. This result suggests that the storage capability of our device is significantly enhanced as the concentration of the CdSe NPs increased due to the increasing trap sites.

Table 1 summarizes the memory window (ΔV) and charge density (Q) of our device (the CdSe concentration: 2.0×10^{15} particles/ml) as a function of amplitude of the applied positive or negative V_{GS} stress. The *C–V* curve shifted to negative direction when the V_{GS} of −20 and −30 were applied for 1 s. On the other hand, it shifted back to positive direction when erasing the memory by applying a V_{GS} of +40 V for 1 s. The memory window (ΔV) at each applied V_{GS} was measured with a capacitance of 15.2 pF. The ΔV was found to be 4.364 and 8.601 V at V_{GS} of −20 and −30 V, respectively. This negative ΔV upon applying negative V_{GS} is attributed to the positive charging of CdSe NPs. The positive charges on the CdSe NPs, on the other hand, were able to return to the pentacene layer by applying positive V_{GS}. The charge density (Q) confined within CdSe NPs can be estimated from the equation $Q = C\Delta V$, where C is the capacitance between gate and the CdSe NPs and ΔV is memory window. As confirmed by our TEM analysis, CdSe NPs were uniformly distributed in the PMMA layer. Provided that all the CdSe NPs were positioned in the midst of the PMMA layer, and each charge occupies one CdSe NP, the charge density (Q) of the memory device, fabricated from 2.0×10^{15} particles/ml of CdSe NPs, was estimated to be 28.86×10^{10} and 57.11×10^{10} electron/cm^2 at the V_{GS} of −20 and −30 V, respectively.

Table 1
The memory window (ΔV) and charge density (Q) with concentration of 2.0×10^{15} particles/ml CdSe NPs as a function of amplitude of the applied positive or negative V_{GS} stress.

	V_{GS} stress			
	Initial	−20 V	−30 V	+40 V
V [V] at 15.2 pF	−1.312	−5.658	−9.913	−2.942
ΔV [V]	–	4.346	8.601	1.63
Q [electron/cm^2]	–	28.86×10^{10}	57.11×10^{10}	10.82×10^{10}

In nonvolatile memory devices, the charge retention capability is one of the most critical factors in determining the device reliability because the data retention properties are often used to estimate

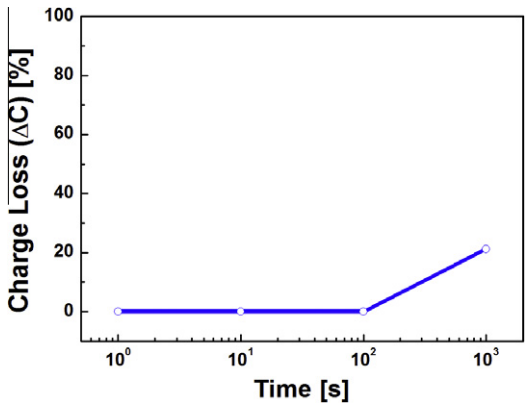

Fig. 4. Retention characteristics in terms of the charge loss (ΔC) after applying −30 V gate stress voltage for 1 s.

the length of time that information can be stored. The charge retention characteristics of the devices fabricated with CdSe NPs were measured from the time-dependent capacitance change after programming at room temperature (Fig. 4). After programming with a V_{GS} of −30 V for 1 s, the ΔC was measured at V_{GS} = 0 V by sweeping the V_{GS} from 2 to −2 V in order to minimize the read disturbance. The charge loss (ΔC) for the device after programming slightly occurred after 10^2 s, and consequently a loss of 21.16% was observed after 10^3 s. While the gradual degradation is apparently not negligible, which may be ascribed to the long-term instability of an organic semiconductor and insulator layers in the transistor memory devices, this observation demonstrates that our NP-based approach can be potentially useful for non-volatile memory applications. Further work is currently being underway to improve the charge retention capability.

4. Conclusions

We demonstrated the use of a CdSe NPs/polymer blend as a tunneling layer in non-volatile organic memory device. The charging and discharging behaviors of CdSe NPs were monitored by the capacitance–voltage analysis of MIS structure, revealing that the sufficiently large memory window and retention characteristics can be achievable in our device. Capacitance shift was observed as a function of increasing applied positive or negative gate voltage stress, which is indicative of successive charging and discharging events within the CdSe NPs via hole injection. We believe that our study may open up the feasibility of NPs floating gate organic memory device in the development of flexible organic devices.

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